

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (original): A reliability evaluation test apparatus which tests a reliability of a semiconductor wafer on the basis of a test signal from a measurement unit, comprising a measurement section and a storage section which has a hermetic and heat insulating structure, stores a semiconductor wafer that is totally in electrical contact with a contactor, and transmits/receives a test signal to/from the measurement section, comprising:

a pressure mechanism which presses the contactor in the storage section; and

a heating mechanism which heats the semiconductor wafer that is totally brought into contact with the contactor by the pressure mechanism to a predetermined temperature,

wherein the reliability evaluation test apparatus evaluates reliability of a multilayered interconnection and an insulting film, which are formed on the semiconductor wafer, under an accelerated condition.

Claim 2 (original): A reliability evaluation test apparatus according to claim 1, wherein the storage section has a table which has a heat insulating structure and on which the semiconductor wafer is placed, a connection ring which surrounds the table and comes into electrical contact with the contactor, and a wiring board which comes into electrical contact with the connection ring and transmits/receives the test signal to/from the measurement section.

COPY

Claim 3 (original): A reliability evaluation test apparatus according to claim 2, further comprising, on the connection ring, a seal member which comes into contact with the

contactor to seal a space in the storage section from an outside, and means for supplying an inert gas and/or reducing gas into the storage section.

Claim 4 (original): A reliability evaluation test apparatus according to claim 1, wherein the pressure mechanism comprises a pressure plate which presses the contactor, a bellows whose lower end is connected to the pressure plate, a support which is connected to an upper end of the bellows and can move vertically, and means for supplying a gas into a space formed by the pressure plate, the bellows, and the support.

Claim 5 (original): A reliability evaluation test apparatus according to claim 1, wherein the heating mechanism comprises a heater which uniformly heats an entire surface of the semiconductor wafer from a lower surface side and also serves as the table.

Claim 6 (original): A reliability evaluation test apparatus according to claim 5, wherein the heater comprises a first heater which heats a central portion of the semiconductor wafer, and a second heater which surrounds the first heater and heats an outer edge portion of the semiconductor wafer.

Claim 7 (original): A reliability evaluation test apparatus according to claim 5, wherein the heating mechanism comprises an auxiliary heater which heats the entire surface of the semiconductor wafer from an upper surface side.

COPY

Claim 8 (original): A reliability evaluation test apparatus according to claim 1, wherein the measurement section comprises an electromigration measurement section and a leakage current measurement section.

Claim 9 (original): A reliability evaluation test apparatus according to claim 8, further comprises a switching mechanism which alternately switches between the measurement sections.

Claim 10 (original): A reliability evaluation test apparatus according to claim 8, wherein the electromigration measurement section comprises a function of supplying three kinds of currents including a DC current, a pulse DC current, and an AC current.

Claim 11 (currently amended): A reliability evaluation test apparatus according to claim 1, in which a plurality of test patterns [[77]] are formed on the semiconductor wafer, and which comprises a test pattern grouping function of putting the plurality of test patterns into groups and executing a reliability evaluation test for not less than five groups simultaneously.

Claim 12 (original): A reliability evaluation test apparatus according to claim 1, further comprising an anisotropic conductive film between the contactor and the semiconductor wafer.

COPY

Claim 13 (original): A reliability evaluation test apparatus according to claim 1, wherein the measurement section simultaneously executes a reliability evaluation test of not less than 100 semiconductor devices formed on the semiconductor wafer.

Claim 14 (original): A reliability evaluation test apparatus according to claim 1, wherein the storage section comprises a heat insulating structure which maintains the semiconductor wafer at a temperature of not less than 160°C.

Claim 15 (original): A reliability evaluation test apparatus according to claim 1, wherein the contactor includes a heat-resistant substrate, and a thermal expansion coefficient of the heat-resistant substrate is 1 to 50 ppm/°C.

Claim 16 (original): A reliability evaluation test system comprising: an aligner which totally brings a contactor into contact with a semiconductor wafer; a transfer tool which transfers the contactor and the semiconductor wafer, which are totally kept in contact with each other by the aligner; and a reliability evaluation test apparatus of claim 1, which executes a reliability evaluation test of the semiconductor wafer transferred by the transfer tool.

Claim 17 (original): A reliability evaluation test system according to claim 16, which allows data communication between the aligner and the reliability evaluation test apparatus.

COPY

Claim 18 (original): A reliability evaluation test system according to claim 16, wherein the aligner includes a microscope to observe the semiconductor wafer on the basis of a test result of the semiconductor wafer.

Claim 19 (original): A reliability evaluation test system according to claim 16, wherein the transfer tool includes a magnet to integrate the contactor and the semiconductor wafer.

Claim 20 (original): A reliability evaluation test system according to claim 16, wherein the transfer tool includes a magnetic circuit and switch means for turning on/off the magnetic circuit, and the switch means excites/degausses the magnetic circuit to cause the transfer tool to attract/release the contactor and the semiconductor wafer.

Claims 21-31 (canceled)

COPY